Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (Currently Amended) An inductor in an integrated circuit, comprising:

a conductive trace disposed over an insulating layer, said insulating layer overlying a semiconductor substrate of a first conductivity type; and

at least two deep wells of opposite conductivity type in said substrate underneath said [[track]] trace, wherein said deep wells are continuous for at least 1.5 μm approximately from a surface of said substrate underneath said insulating layer.

2. (Original) The inductor of claim 1 wherein said conductive trace comprises metal.

3. (Original) The inductor of claim 1 wherein said semiconductor substrate is a p-type substrate and said deep wells are n-type wells

4. (Original) The inductor of claim 1 wherein said semiconductor substrate is an n-type substrate and said deep wells are p-type wells.

5. (Original) The inductor of claim 1 wherein said deep wells are not reverse biased.

6. (Original) The inductor of claim 1 wherein said deep wells are arranged in a pattern to form a substantial depletion space in said substrate underneath said trace.

7. (Original) The inductor of claim 1 wherein said deep wells are cuboid.

8. (Original) The inductor of claim 1 wherein said deep wells are L shaped cuboid.

9. (Canceled)

10. (Canceled)

11. (Original) The inductor of claim 1 wherein said deep wells are formed by ion implantation.

12. (Original) The inductor of claim 11 wherein said ion implantation comprises a first stage in which ions are accelerated to a first energy level and at least a second stage in which ions are accelerated to an energy level different from said first energy level.

13. (Original) An inductor in an integrated circuit, comprising:

a conductive trace disposed over an insulating layer, said insulating layer overlying a semiconductor substrate of a first conductivity type;

a shallow trench isolation region, formed in said substrate underneath said trace; and

at least two deep wells of opposite conductivity type in said substrate underneath said shallow trench isolation region.

14. (Original) The inductor of claim 13 wherein said conductive trace comprises metal.

15. (Original) The inductor of claim 13 wherein said shallow trench isolation comprises silicon dioxide.

16. (Original) The inductor of claim 13 wherein said semiconductor substrate is a p-type substrate and said deep wells are n-type wells.

17. (Original) The inductor of claim 13 wherein said semiconductor substrate is an n-type substrate and said deep wells are p-type wells.

18. (Original) The inductor of claim 13 wherein said deep wells are not reverse biased.

19. (Original) The inductor of claim 13 wherein said deep wells are arranged in a pattern to form a substantial depletion space in said substrate underneath said trace.

20. (Original) The inductor of claim 13 wherein said deep wells are cuboid.

21. (Original) The inductor of claim 13 wherein said deep wells are L shaped cuboid.

22. (Original) The inductor of claim 13 wherein said deep wells are continuous.

23. (Original) The inductor of claim 22 wherein said deep wells are continuous for at least 1.5 μm approximately from a plane in said substrate underneath and adjacent to said shallow trench isolation region.

24. (Original) The inductor of claim 13 wherein said deep wells are formed by ion implantation.

25. (Original) The inductor of claim 24 wherein said ion implantation comprises a first stage in which ions are accelerated to a first energy level and at least a second stage in which ions are accelerated to an energy level different from said first energy level.

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Canceled)

41. (Canceled)

42. (New) An inductor in an integrated circuit, comprising:

a conductive trace disposed over an insulating layer, said insulating layer overlying a semiconductor substrate of a first conductivity type; and

at least two deep wells of opposite conductivity type in said substrate underneath said trace, wherein said deep wells are not reverse biased.